Upgrade to the front-end electronics of the BESIII muon identification system

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Resistive Plate Chambers (RPCs) built from a new type of Bakelite developed at Institute of High Energy Physics (IHEP), Chinese Academy of Sciences have been used in the BESIII Muon identification system for several years without linseed oil coating, but characteristic aging performances were observed. To adapt to the RPCs in the aging state, the front-end electronics have been upgraded by enhancing the front-end protection, improving the threshold setting circuit, and separating power supplies of the comparator and the field programmable gate array (FPGA). Improvements in system stability, front-end protection and threshold consistency have been achieved. In this paper, the system upgrade and the test results are described in detail.

Keywords: BESIII, Upgrade, Resistive Plate Chamber, Front-end protection

I. INTRODUCTION

Resistive Plate Chamber (RPC) is a gaseous detector widely used in many high energy physics experiments, such as the B-factory experiments (BaBar at SLAC and Belle at KEK), the LHC experiments (ALICE, ATLAS, CMS) and the ARGO cosmic ray experiment at Yangbajing in Tibet, China [1–9]. The resistive material and surface smoothness of the resistive plate are critical for a good RPC. Differing from the glass electrodes in Belle or the bakelite plates with linseed oil treatment in BaBar, the resistive material of electrodes used in the RPC for the muon identification system of Beijing Spectrometer (BESIII) is a special type of phenolic laminate [10]. Surface quality of these laminates is superior to other bakelite plates used to construct RPCs elsewhere. However, like other gaseous detectors, the BESIII-type RPCs working in streamer mode also suffer from aging problems [11]. The aging effect causes declining efficiency of the detectors and failure of the electronics. Thus, it is necessary to upgrade the electronics to achieve high stability and reliability needed for the BESIII muon identification system.

In this paper, we report our work on upgrading to the front-end electronics of the BESIII muon identification system, focusing on the possibility of using two stages of the back-to-back protection diode (BBPD) for the streamer mode working RPCs, and on the method of how to improve the threshold consistency. After installation of the upgraded electronics, the test results show that the goals of higher stability and reliable front-end protection are achieved, and the threshold consistency is improved as expected.

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II. UPGRADES TO THE RPC ELECTRONIC SYSTEM

A. Enhancing the front-end protection

The original FECs is of one stage of BBPD with a $20\,\Omega$ resistor to prevent possible sparks from RPCs, but this one-stage design fails to protect the circuit effectively. Sometimes, the strips of RPCs generate abnormally large signals at the moment of beam loss because of the high sensitivity of the RPC detectors. In presence of these large input signals, the output after one stage of BBPD remained high enough to damage the comparator. To provide better protection, the one stage of BBPD was upgraded to two stages of BBPD [12], as shown in Fig. 1. The two stages of BBPD were expected to reduce the abnormally large signal amplitude to a safe level without affecting normal small signals or the efficiency of the RPC detector. This circuit was simulated using PSpice. A schematic of this simulation is shown in Fig. 2.
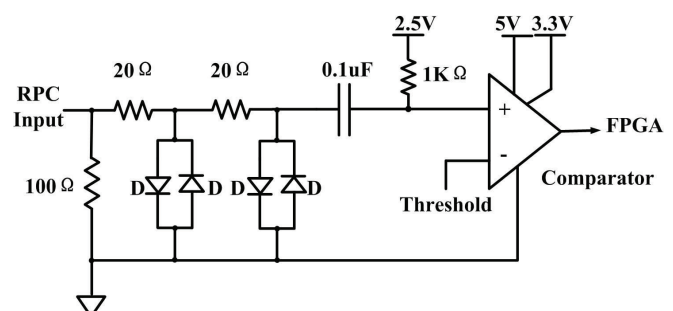

Fig. 1. Front-end protection circuit with two BBPD stages.

Table 1 shows the results of a simulation of one and two stages of BBPD with small input signals and large input signals, which are both likely to appear in the real RPC output. The results show that, for large input signals, the output am-

TABLE 1. Simulation results

	Signal type	Input	Output	Atenuation coefficient (Input-output)/Input	Transmission coefficient Output/Input
One stage of BBPD	Small signal input	$-58\,$mV	$-56\,$mV	3.4%	96.6%
		$-100\,$mV	$-98\,$mV	2.0%	98.0%
	Large signal input	$+710\,$V	$+30\,$V	95.8%	4.2%
		$-690\,$V	$-29\,$V	95.8%	4.2%
Two stages of BBPD	Small signal input	$-58\,$mV	$-55\,$mV	5.2%	94.8%
		$-100\,$mV	$-95\,$mV	5.0%	95.0%
	Large signal input	$+710\,$V	$+2\,$V	99.7%	0.3%
		$-690\,$V	$-2\,$V	99.7%	0.3%

Fig. 2. (Color online) Simulation scheme.

Fig. 3. Threshold setting circuit.

plitudes after one stage of BBTD are $30\,$V and $-29\,$V, being still high enough to damage the comparator. The two stages of BBPD, with the outputs of $2\,$V and $-2\,$V, are capable of protecting the comparator from large signals. For small input signals, the diode junction capacitance is somewhat small (about $2\,$pF for a diode in MA3J147 used in BBTD), so the two stages of BBDP show only little more attenuation than one BBDP stage, which does not affect the efficiency of the RPC detector significantly. These results of the simulation indicate that two stages of BBDP can be used in the FECs.

B. Improving the threshold setting circuit

Both the high RPC voltage and FEC threshold contributed to the RPC efficiency. We lower the high voltage to avoid RPC and FEC failure, and lower the FEC threshold to maintain the RPC efficiency. In this way, the FEC threshold was expected to have a low relative error, especially at low thresholds. This would guarantee the consistency of the threshold for all the 572 FECs used in the BESIII.

The original FEC threshold setting circuit is shown in Fig. 3(a). It consists of a DAC, an emitter follower, and a comparator. As the input signal of comparator is pulled up to V_{DC}, the corresponding threshold can be calculated as:

$$V_{\mathrm{TH}} = V_{\mathrm{DC}} - V_{\mathrm{DAC}} = V_{\mathrm{DC}} - DV_{\mathrm{REF}}/256, \qquad (1)$$

where, V_{DC} is comparator pull-up voltage ($2.5\,$V), V_{DAC} is the DAC output voltage, D is the DAC setting code, and V_{REF} is
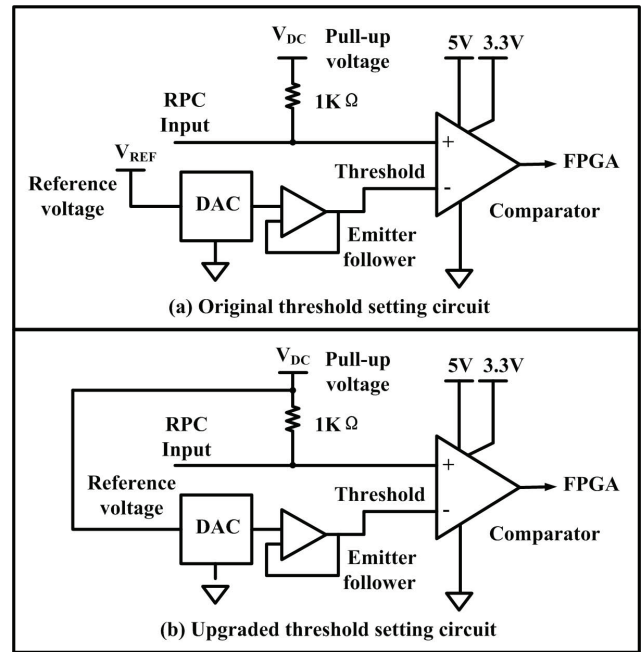
the DAC reference voltage ($2.5\,$V). The original FECs used a voltage regulator for the pull-up voltage and another regulator diode for the DAC reference voltage. Considering the integral nonlinearity (INL) of the DAC and accuracy of each regulator, the worst absolute error of the corresponding threshold can be calculated by Eq. 2,

$$\sigma_{V_{\mathrm{TH}}} = \sqrt{(\sigma_{V_{\mathrm{DC}}})^2 + \frac{1}{256^2}D^2(\sigma_{V_{\mathrm{REF}}})^2 + \frac{1}{256^2}(V_{\mathrm{REF}})^2(\sigma_D)^2}. \tag{2}$$

The INL of the DAC is $\pm 1/2$ LSB and the accuracy of each regulator is 1%. The absolute error of the corresponding threshold as a function of DAC code is shown in Fig. 4. When the threshold is set to a low value, such as $48.8\,$mV (DAC code 251), the absolute error is $35.1\,$mV and the relative error is 72%, which are apparently unbearable.

The problem is solved by using a single regulator for both comparator pull-up and DAC reference voltage [13]. In the upgraded threshold setting circuit, shown in Fig. 3(b), the threshold can be calculated by Eq. 3,

$$V_{TH} = V_{DC} - V_{DAC}$$
$$= V_{DC} - \frac{D}{256}V_{REF} \qquad (3)$$
$$= (1 - \frac{D}{256})V_{REF}.$$

The worst absolute error of the threshold can be calculated as:

$$\sigma_{V_{TH}} = \sqrt{(1 - \frac{D}{256})^2(\sigma_{V_{REF}})^2 + (V_{REF})^2\frac{(\sigma_D)^2}{256^2}} \qquad (4)$$

In this case, the absolute error of threshold will be significantly reduced, especially when the threshold is set at a low range, as shown in Fig. 4. Take a threshold of 48.8 mV (DAC code 251) as an example, the worst absolute error in the upgraded threshold setting circuit drops to only 4.9 mV. The thresholds between different FECs vary by no more than the worst absolute error of threshold. Threshold consistency was significantly improved after the upgrade.

Fig. 4. Absolute error of threshold vs. DAC code.

C. Separating power supplies of comparator and FPGA

The data transmission for the RPC front-end readout electronics system is organized in the form of daisy chain, in which the FPGA plays a key role. In the original design of the FECs, due to the regulator supplies 3.3 V voltage both to the comparator and FPGA, once the comparator was damaged, the FPGA couldn't work either, causing the entire data chain to crash. As a precautionary measure to ensure data from other FECs transmitted properly on occurrence of any FEC comparator failure, the comparator and the FPGA were upgraded to use separate powers.

III. TESTS AND INSTALLATION

A. Test of front-end protection

The front-end protection circuit was tested to determine whether the two stages of diodes were suitable for the upgrade [14]. To assess the protection for large signals, input signals of 710 V and −690 V amplitudes were fed as input into the two BBDP stages, as shown in Fig. 5 (Ch1). The output signals of the two stages showed amplitudes of 2.2 V and −3.2 V, respectively, shown in Fig. 5 (Ch2). The comparator exhibited no failure for such large input pulses. Concerning small signals, two pulses with amplitudes of −58 mV and −100 mV served as input to the double BBDP stage, as shown in Fig. 6 (Ch1). The observed pulse amplitudes at the output of the protection circuit were −54 mV and −95 mV, respectively, also shown in Fig. 6 (Ch2). The values were consistent with our simulation, giving the desired attenuation for large signals while minimally attenuating small ones. The results indicated that the upgrade of the front-end protection was effective and appropriate.
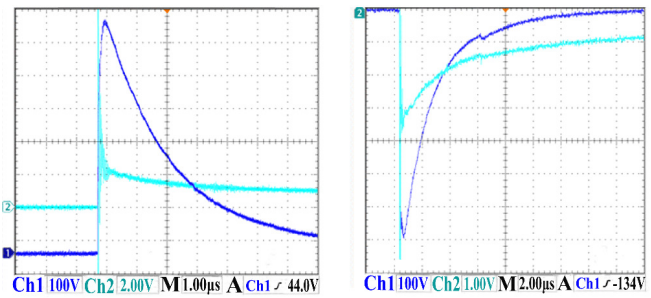

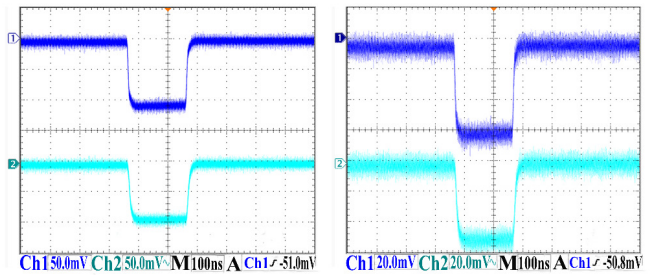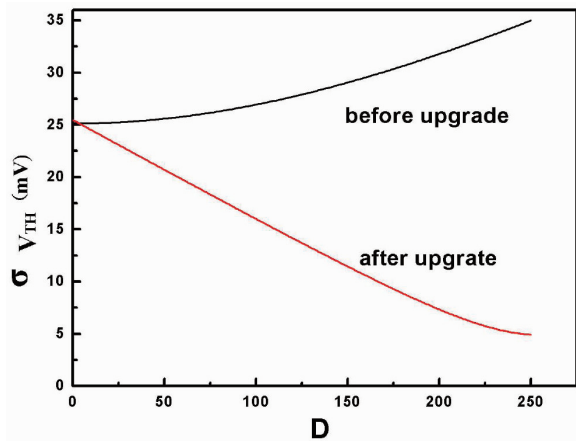Fig. 5. (Color online) Waveforms for large input signals.

Fig. 6. (Color online) Waveforms for small input signals.

B. Test of FEC threshold consistency

This test involved a random selection of 15 FECs from 700 candidate FECs and analysis of the variation in thresholds between different FECs with the DAC codes set at 252, 251 and 250 [15]. The corresponding threshold value was recorded by measuring the actual threshold value compared to the comparator pull-up voltage on each board. The results are given

TABLE 2. Upgraded FECs threshold consistency test

DAC code	Average $\overline{V}$	Maximum deviation ΔV_{max}	Standard deviation σ
252	41.1 mV	1.87 mV	0.67 mV
251	52.1 mV	1.80 mV	0.63 mV
250	61.7 mV	1.88 mV	0.69 mV

in Table 2. One sees that the difference between these FEC thresholds is about 1% after the upgrade.

C. The RPC cosmic ray test

Figure 7 shows the histograms of a cosmic ray test using (a) the original FECs and (b) the upgraded FECs [16], at the same high-voltage (7.7 kV) and threshold (50 mV) settings. For the original FECs, some channels have unexpectedly more counts, and it appears that the thresholds of these channels were comparatively lower than others. For the upgraded FECs, there are counts in each of the channels but no channels have excessively large counts. This indicates that the threshold consistency is surely improved after the upgrade.
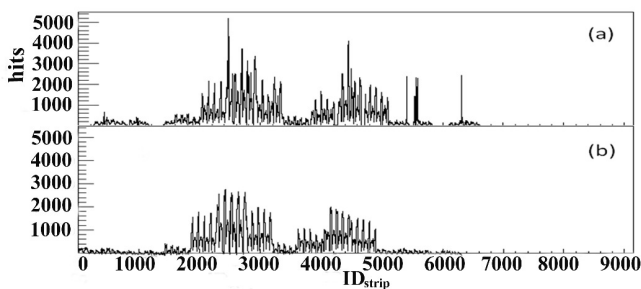

Fig. 7. The histograms of a cosmic ray test.

D. Efficiency and noise test

Tests of efficiency and noise for the RPCs detectors were conducted under the cosmic ray environment after the upgraded FECs installed in the BESIII. As a function of voltage, Fig. 8 shows the efficiency and Fig. 9 shows the noise, for three threshold settings at 40 mV, 50 mV, and 60 mV. The 7.7 kV efficiency of the RPC reached 95–96% at 50 mV threshold while the noise was about 0.08 Hz/cm^2. The results are up to the system indicators, which confirm the upgrade is successful.

IV. INSTALLATION OF UPGRADED FECS

A total of 572 FECs were installed at BESIII in 2011. Because of difficulties in the maintenance of the endcaps, ex-
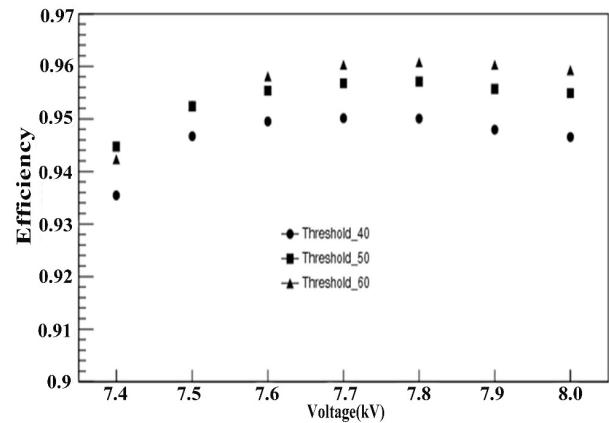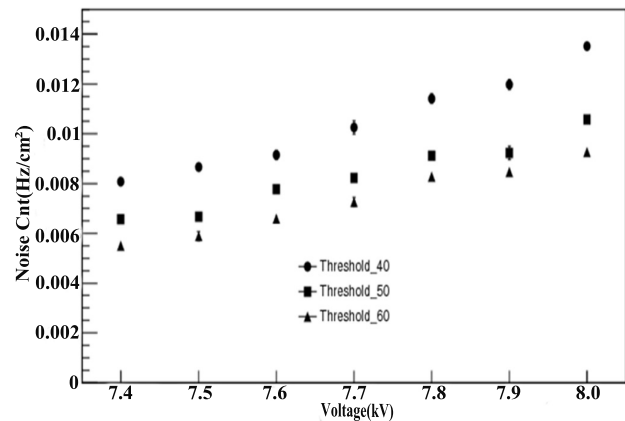

Fig. 8. Efficiency test results.
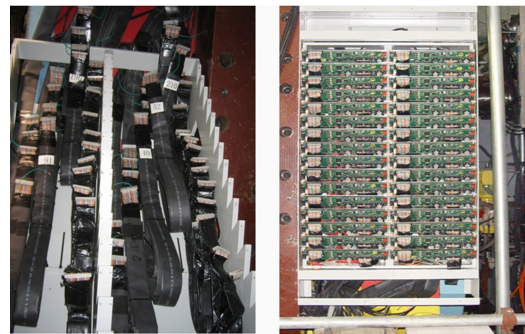

Fig. 9. Noise test results.

Fig. 10. (Color online) Extension cables and the shielded box.

tension cables were used for the FECs in the shielded box adjacent to the spectrometer. This is shown in Fig. 10.

V. CONCLUSION

The RPC FECs were upgraded to produce the high stability and reliability needed for the BESIII muon spectrometer. First, two stages of BBPD were added before the comparator

to prevent FECs from being damaged by the large signals that occur when the RPC sparks. Second, the comparator pull-up and DAC reference voltage were supplied with a single voltage regulator to improve the threshold consistency. At last, the power supplies of the comparator and FPGA were separated to ensure that FPGA continue to work normally even if the comparator was damaged. The upgraded FECs have been constructed and tested. A total of 572 FECs were installed on the BESIII during the summer of 2011. A week-long cosmic ray test has been conducted and the result shows that the upgraded RPC readout electronics meet the requirements of the BESIII.

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